



# SERIAL OUTPUT CONTROLLER

## SOC003 / SOC004

### Features

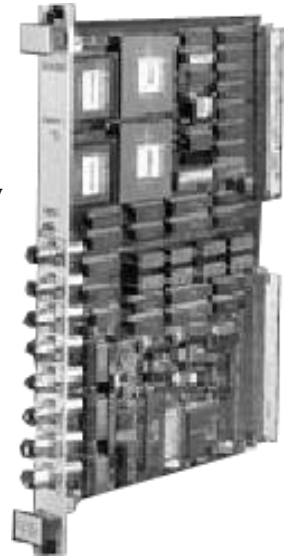
- Bit rate 1 bps through 15 Mbps
- Dual 512 K x 16-bit simulation data memory buffers for real-time simulation
- Output format selectable, 4-to 512 K words / major cycle.
- Output data code IRIG 106 compliant
- Data placed into on-board Ping-Pong buffers, accessed as memory on the bus.
- End of Buffer interrupt - supports continuous (Ping-Pong) output operations.
- TTL Serial data and clock outputs. (Optional RS-422 Outputs)
- VME (SOC003) or ISA (SOC004) Form-factor
  - 13.2" x 4.5". ISA-PC/AT
  - Single Slot 6U x 160mm VME

### General Description

The SOC004, Serial Output Controller, is a full size ISA-PC/AT printed circuit card. The VME version of this device is the SOC003. The same functionality is available from both form-factors.



The Serial Output Controller generates a serial output data stream using either static or dynamically updated data loaded from the data-bus (ISA or VME). With ample memory buffers on-board, any of several modes of data generation may be used. Data is output repeatedly or in bursts. Data to be serialized may be continuously updated by way of the data-bus controller. A frequency synthesizer, resident on the module, allows precise bit rates to be generated



#### SINGLE BUFFER MODE

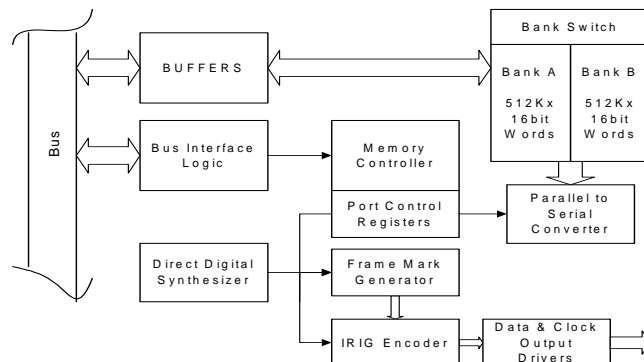
While data is output from buffer A, the alternate buffer B may be loaded with the new data. At the end of the current buffer (A), the SOC will switch to the alternate buffer (B).

#### DUAL BUFFER OUTPUT MODE

The SOC automatically Ping-Pongs between buffers A and B. Alternately, output is derived from a single buffer until released to the other.

#### BURST MODE

If the BURST MODE is selected, the SOC ends the data and clock transmission at the end of the currently selected buffer.





# SERIAL OUTPUT CONTROLER

*SOC003 / SOC004*

## SPECIFICATIONS

### SIGNAL INTERFACES

- Data and Clock
  - 0 deg Clock
  - Clock and Data polarity normal/inverted software selectable.
- TTL w/ BNC Coaxial Connectors
- RS-422 (Option) w/ Twinax Connectors
- External Clock Input
  - 1 Hz-15 MHz range, 50% duty cycle.
- End-of-Block:  
Synchronization pulse signal occurs at end of Data Block Output

### DATA FORMAT

- 4 to 16 bits per word.
- MSB or LSB transmitted first.
- Up to 512K words per major frame.
- Data Codes:
  - NRZ-L, M, S;
  - BiPhase-L, M, S;
  - DM-M, S.

### MEMORY

- Two 512K x 16 bit word buffers in a ping-pong architecture.

### OPERATION

- Selectable buffer output size: 4 to 512K words/buffer.
- Format switching
  - While data is output from one buffer, the alternate buffer may be loaded through ISA bus cycles.- On software command, the memory access controller will automatically switch the data source back to the beginning of the current buffer each time the end of the buffer is reached, or switch to the alternate buffer after the completion of the next word.
- Automatic ping-pong buffer operation at end of buffer output.
- Burst or Continuous mode.
- Selectable constant or gated clock operation for burst output mode.
- End of buffer interrupt.

## Ordering Information

SOC003 Standard Module VME  
SOC004 Standard Module ISA

OPSOC-01 RS-422 I/O

Recognizing that no standard product can meet all the needs of all users, GDP stands ready to provide units tailored to unique applications.

The statements in this data sheet are not intended to create any warranty, expressed or implied. Equipment specifications are subject to change without notice.

300 Welsh Road · Building 3 · Horsham, PA 19044-2273  
Phone: 215-657-5242 Fax: 215-657-5273

URL: <http://www.gdp.space.com>  
E-mail: [gdpinfo@gdp.space.com](mailto:gdpinfo@gdp.space.com)