

# SGLS Test Set

## Model 630

### Features

- ◆ 3 Operational Modes
  - ◆ SGLS Ternary BERT
  - ◆ Serial data BERT
  - ◆ SGLS Command Processor
- ◆ Test 4 Command Rates
  - ◆ 1 kbps & 2 kbps (Std)
  - ◆ Other Rates (optional)
- ◆ Independent Transmit and Receive
- ◆ Six Pseudorandom Data Patterns
  - ◆ 2<sup>7</sup>, 9, 11, 15, 20, 23<sub>-1</sub>
  - ◆ Forward and Reverse
- ◆ Programmable Fixed Pattern
  - ◆ 24 or 32 Bits (Binary Mode only)
- ◆ Differentially Encoded Ternary
- ◆ Receive Data Prediction
  - ◆ Eliminates Doublet Errors
- ◆ Tests ability of SGLS Receiver to deal with timing variations
- ◆ Reports Errors on 1, 0 and S Independently and as a group
  - ◆ Front Panel Display
  - ◆ Remote Control Reporting
- ◆ Integrated SGLS Modulator and / Or Demodulator (Optional)
- ◆ Remote Control & Monitoring
  - ◆ RS-232 (Standard)
  - ◆ IEEE-488 (Optional)
  - ◆ Ethernet (Optional)

### General Description

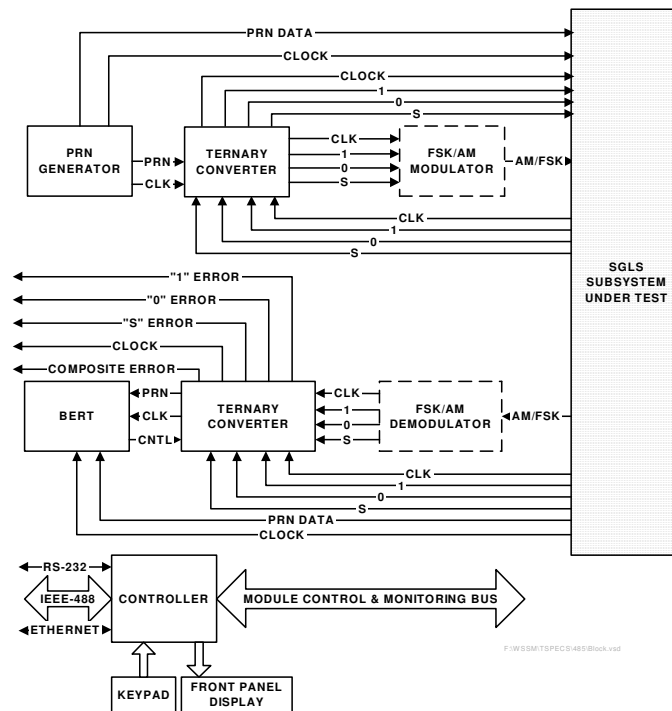
The model 630 is an assemblage of functional elements that are configured to assist the design and production engineer in testing data links. The model 630 provides signaling interfaces that allow testing using serial pseudo-random data on a standard PCM data link or SGLS Command Link.

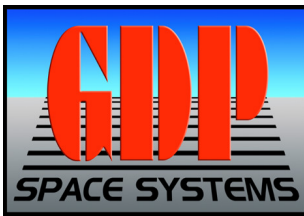


To test a SGLS Command Link using an external AM/FSK modulator, the model 630 supplies the 1, 0, and S signals. Optionally, a GDP AM/FSK modulator is included in the unit. In that case the modulated baseband signal is provided for use in the system under test. The return link signaling is a similar construct. Either the ternary or AM/FSK signals are used.

A user selected pseudorandom data sequence is encoded to produce the ternary signaling needed for the SGLS data link. Using this technique, all three signaling elements are tested and error reports generated to identify weakness in the individual lines.

Independent transmit and receive sections permit the up-link to be operated at a different data rate from the down-link.





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### SPECIFICATIONS

#### Inputs:

- ◆ PRN Data & Clock
- ◆ AM/FSK (0.1 to 5.0 Vp-p) [Option]
- ◆ SGLS 1, 0, & S

#### Outputs:

- ◆ PRN Data & Clock
- ◆ AM/FSK (-30 to +10 dBm) [Option]
- ◆ SGLS 1, 0, & S
- ◆ Error Reports 1, 0, S, Syntax & Composite

#### Test Data Patterns:

- ◆ PRN 2<sup>7, 9, 11, 15, 20, 23</sup>-1; Fwd & Rev.
- ◆ Fixed Pattern (24, 32 bits)

#### Data Rates:

- ◆ SGLS (1 & 2 kbps Standard)  
Other rates Optional
- ◆ PCM PRN Data (up to 25 Mbps)

#### SGLS FSK Tones:

- ◆ 95 kHz, 76 kHz, 65 kHz  
Other frequencies optional

#### SGLS AM Triangle:

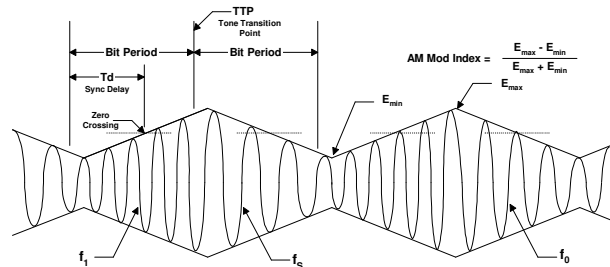
- ◆ 500 Hz, 1 kHz, 5 kHz (Standard)
- ◆ Modulation Index: 0.33 to 1.0

#### AM Generator Bit Synchronization:

- ◆ Phase programmable in 0.1% increments of the bit period.
- ◆ Clock-Rate adjustable +/- 5%

#### Unique SGLS Test Methods:

- ◆ Cycling S, 0, & 1
- ◆ Cycling S, 0, & 1 with selectable gaps of 100, 200, 300 or 50ms every 100ms
- ◆ Cycling Fixed Pattern
- ◆ Continuous S, 0 or 1
- ◆ Sweep AM Phasing relative to FSK
- ◆ Command String Input / Output via Remote Control Port
  - ◆ 32 kbyte Input Buffer
  - ◆ 32 kbyte Output Buffer
  - ◆ Larger buffer sizes available
- ◆ Remote Control Interfaces
  - ◆ RS-232 (Standard)
  - ◆ IEEE-488 or Ethernet (Optional)



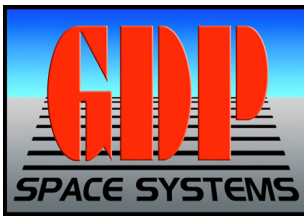
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### Ordering Information

MD630-00	Basic Unit	OP630-16	Expanded Cmd Buf (> 32k)
OP630-03	Special Data Rate		(OP-16 also Requires OP-15)
OP630-11	EtherNet Remote Control	OP630-20	Add SGLS Modulator
OP630-15	Command Processor	OP630-30	Add SGLS Demodulator
OP630-10	IEEE-488 Remote Control	OP630-40	Special I/O
		OP630-45	DiBit Input
		OP630-46	DiBit Output

Recognizing that no standard product can meet all the needs of all users, GDP stands ready to provide units tailored to unique applications.

The statements in this data sheet are not intended to create any warranty, expressed or implied. Equipment specifications are subject to change without notice.

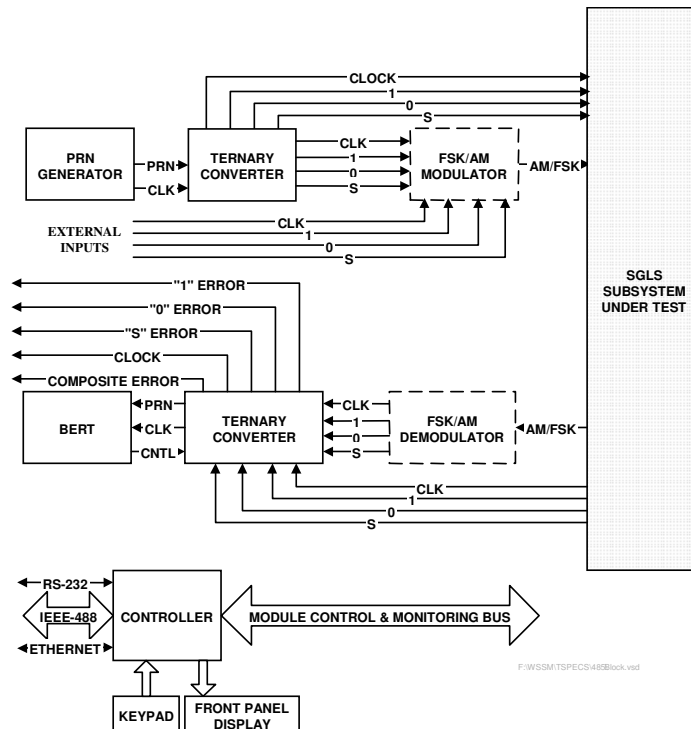


# Ternary BERT Function

The Ternary BERT Function of the Model 630 offers the user the Bit Error Rate (BERT) testing capabilities normally found only in a communication link BERT. The primary mode of operation utilizes a selectable length Pseudo Random Number (PRN) generated bit sequence that is converted into a series of SGLS ternary (S, 0, 1) tones. The use of a PRN sequence to generate the ternary data is an exciting new feature that provides the same quality of testing normally used in serial data communication links. Selectable PRN sequence lengths of  $2^{7, 9, 11, 15, 23} - 1$  bits in forward or reverse direction are provided. The tester also allows the use of a programmable 24 bit fixed pattern as the source of the ternary data. The ternary data is encoded in a predictable manner which eliminates doublet errors. Other unique SGLS test methods provided include a recycling S, 0, 1 pattern, a recycling S, 0, 1 pattern with a gap of 100us, 200us, 300us or 50msec inserted every 100msec and a continuous S, 0, or 1.

The ternary data can be transmitted and received as baseband S, 0, 1 data or with the optional Modulator and Demodulator the complete SGLS FSK/AM waveform can be generated and received. The SGLS FSK tones are generated at the standard 65k Hz, 76k Hz and 95k Hz frequencies or they can be programmed to any other set of frequencies up to 3M Hz.

The transmit and receive functions are totally independent, which allows variable delays in the data path to be transparent. Individual error pulse outputs are provided for the S, 0, and 1 signals as well as a composite error pulse. Processed error reporting includes: an error count for each test and an average Bit Error Rate (BER).



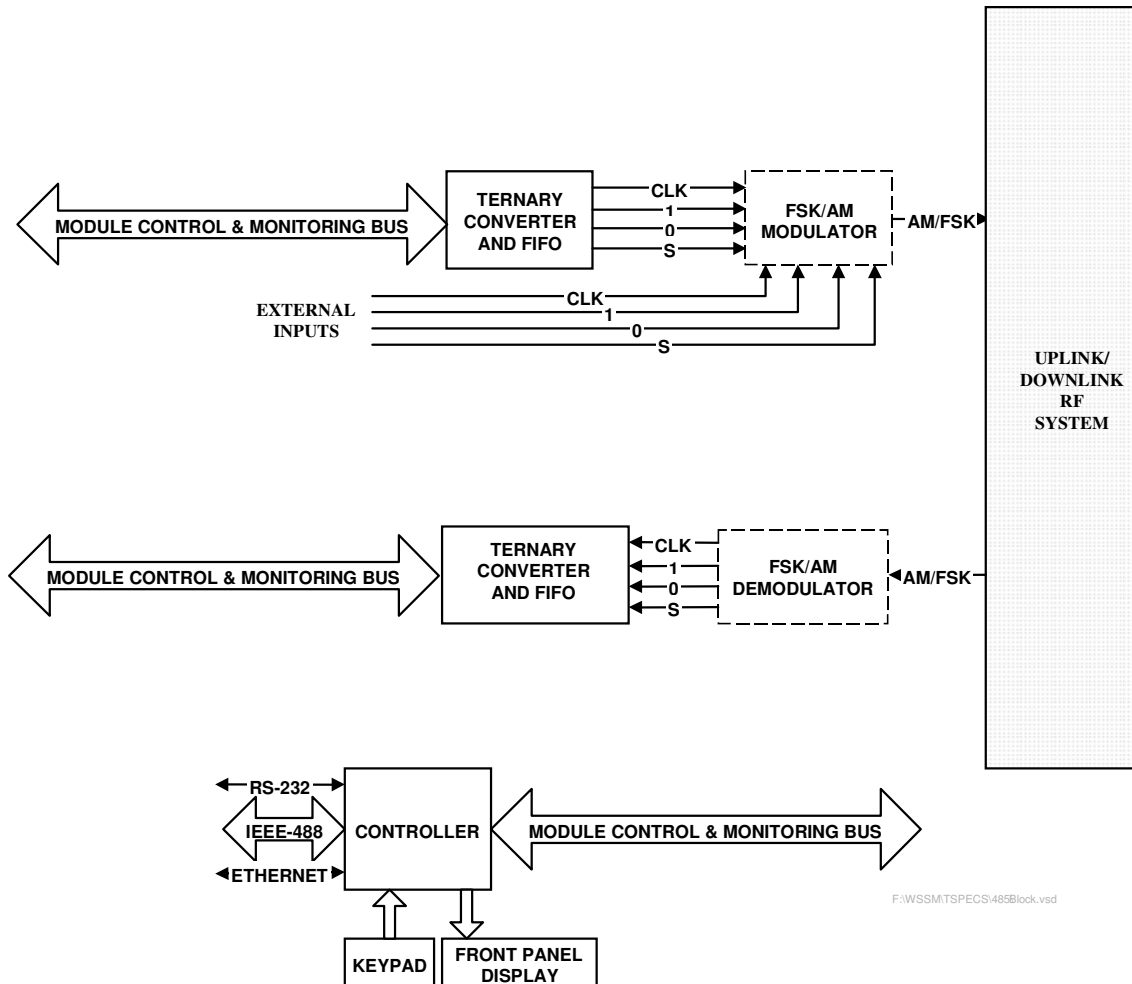


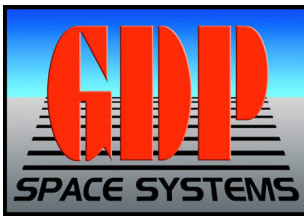
# Command Processor Function

The Command Processor function of the Model 630 allows the user to send uplink command sets to the satellite and receive command echo returns from the antenna system for verification.

Command sequences can be downloaded from a host computer and stored in the Model 630 processor memory via the remote control interface. When the command sequence is initiated, the stored commands are generated and the ternary data is output via a FIFO to the AM/FSK modulator. Alternatively, ternary data (S, 0, 1) can be input directly from an external source to the modulator. The SGLS AM/FSK waveform produced by the modulator is output to an uplink transmitter. The return echo from a downlink receiver is demodulated by the AM/FSK demodulator and the resulting base-band ternary data sent to a host processor for verification.

In a test mode the modulator output can be looped back to the demodulator at the near end or far end.





# BINARY BERT Function

The Binary Bit Error Rate Tester (BERT) fills the need for high performance link verification and qualification. The user is provided with totally independent transmit and receive functions to allow rapid fault isolation and data link characterization through a real-time bit-contiguous test. Features such as an internal DDS frequency synthesizer and IRIG Code converter make the Model 630 especially suited to the test and evaluation of PCM Telemetry data link systems and components.

Test results available are: Accumulated Bit Errors, Measured Bit Error Rate, Accumulated Block Errors, Accumulated Error-free Seconds, Accumulated Error Seconds, Measured error Symmetry, Accumulated Bit Count Integrity loss (Bit Slips), Measured Transmit and Receive clock rate.

The Model 630 BERT has the capability of outputting and testing forward and reverse PRN patterns of  $2^7-1$ ,  $2^9-1$ ,  $2^{11}-1$ ,  $2^{15}-1$ ,  $2^{20}-1$ ,  $2^{23}-1$ . It also can output and test a repeated 24 bit or 32-bit pattern. User defined sequences can be sent if they are 24 or 32 bits long or a sub-multiple of 24 or 32 bits. The host sends the bit sequence over the remote control link as a box setup command string that is loaded into a setup register on the card. They can also be loaded from the front panel. The unit will then continually output that 24 or 32 bit sequence and report errors.

