



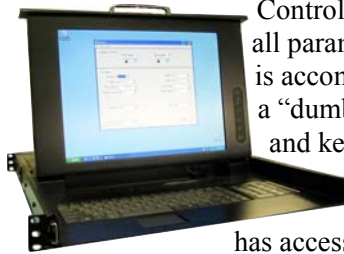
Multi-Channel PCM BIT SYNCHRONIZER Model 2365

Features

- ◆ Up to 4-Channels in 1U
- ◆ Bit Rates:
 - 5 bps to 20 Mbps
 - 5 bps to 40 Mbps (Opt)
- ◆ Performance within 1 dB of theory
- ◆ Loop Bandwidth Settings from 0.01% to 1.6%
 - Extended LBW Range (Opt)
- ◆ NRZ-L/M/S, BiØ-L/M/S, DM-M/S; MDM-M/S
- ◆ Randomizer/Derandomizer
- ◆ Scrambler/Descrambler
 - CCITT V.35/36
- ◆ Viterbi Decoder
- ◆ Frame Pattern Detector
- ◆ Input Signal Status
 - Sync and Loss
 - Measured Bit Rate
 - Bit Rate Deviation
 - Measured Signal Level
 - Input Data Polarity
- ◆ Signal/Data Quality Status
 - Eb/No Measurement
 - Frame Sync Pattern Error Count (BER Status)
 - Viterbi Error Count
 - BERT/ PRN BER Measurement
- ◆ Date Generator/Simulator
 - Serial and QPSK(Opt)
- ◆ Advanced Lock Detection
- ◆ Auto Bit-Rate Scan (Opt)
- ◆ OPSK/OQPSK/SOQPSK Resequencer (opt)
- ◆ Remote Control via
 - Ethernet
 - RS-232
 - IEEE-488, (Opt)
- ◆ 1.75-inch High Chassis

General Description

The GDP Model 2365 Multi-Channel PCM Bit Synchronizer houses up to 4 high-performance bit synchronizer channels in a 1U chassis. The optimized digital design of this unit affords the highest performance characteristics currently available.



Control and monitoring of all parameters and features is accomplished by way of a “dumb” terminal, mouse and keyboard or a remote computer. The remote computer

has access to the unit through an Ethernet interface, RS-232 or IEEE-488 interface.



The bit synchronizer is capable of maintaining synchronization to -3 dB Eb/No at signal levels as low as 0.1 Vpp. Search acquisition is attainable in less than 50 bits and synchronization is maintained for a period of at least 256 bit periods without a transition.

Four Analog inputs are provided per channel. Optional digital inputs for RS-422 and TTL levels may be included. Each channel presents a variety of outputs to support complex system requirements.

A standard IRIG randomizer/derandomizer (forward and reverse) is included as is a CCITT V.35 and V.36 scrambler/descrambler. A variety of Viterbi decoders are available including R1/2 K7 (Std), R3/4 K7 and R1/3 k7 (please inquire for other FEC options). Reed Solomon Decoding is an available option.

Automatic Polarity Correction (APC) and an additional level of synchronization assurance is provided by invoking the Frame Pattern Detector.

Data-stream quality is measured and reported to the user in the form of: Eb/No, Frame Synch Pattern Errors, Viterbi Decoder Errors, Bit Error Rate.

A data stream generator / simulator is included to facilitate system testing.

An Auto Scan feature is available that allows the bit synchronizers to scan the input for up to 8 pre-selected bit rates, input codes and frame patterns. When an acceptable signal is present, the Bit Synchronizer automatically locks to it and recovers the data and clock. Should this signal drop-out, the bit synchronizer re-initiates the scan sequence.



Multi-Channel PCM BIT SYNCHRONIZER Model 2365

SPECIFICATIONS

Inputs, each Bit Sync Channel

Analog Inputs 2 Inputs per Bit Sync- 50 ohms (optional 75) or High Z Digital Inputs
Differential RS-422 and TTL (Optional)

Performance

Bit Rate Range 5bps to 20 Mbps (40 Mbps Optional)
Tuning Resolution X.XXXE^N (1≤N≤7)
Input Levels 0.1 Vpp Min., +/- 12 V Max.. (others available)
DC Offsets 100% of the input peak-to-peak signal level.
AC Offset No degradation up to 100% of input signal amplitude at 0.1% of the bit rate.
Loop Bandwidths 0.01% to 1.6% (Extended LBW Range Optional)
Acquisition Range 2x LBW
Sync Acquisition Threshold SNR 0 dB
Sync Maintenance SNR -3dB
Sync Acquisition ≤ 50 bits
Sync Retention 256 bits without transitions
Bit Error Rate 1 dB to 40 Mbps

Features

Input/Output PCM Codes NRZ-L/M/S, BIØ-L/M/S, DBIØ-M/S, DM-M/S; MDM-M/S
Randomizer/Derandomizer IRIG 106 forward and reverse
Descrambler CCITT V.35/V.36
Viterbi Decoder R 1/2, K 7 with G1/G2 Swap and G2 Invert, (others available)
Resequencer QPSK/OQPSK/SOQPSK (Optional)
Frame Pattern Detector Up to 64 bits with programmable strategy and APC
Auto Scan (Optional) Up to 8 preset: Bit Rate, Code, Frame pattern per Bit Sync
Output Data Polarity Input polarity Normal / Inverted.
Output Clock Phase 0, 90, 180 & 270 degrees to 20 Mbps; 0 & 180 degrees 20Mbps to 40Mbps
BERT Function Bit-Error-Rate PRN Generator/Error Detector (opt)

Outputs, each Bit Sync Channel

TTL (Each Channel)- Coded PCM and Clock (Programmable 0, 90, 180, 270 degrees)
RS422 (Each Channel)- Coded PCM and Clock (Programmable 0, 90, 180, 270 degrees)
Bipolar Tape Output (Each Channel)- +/-1V - Coded PCM
Lock Status: - Bit Synchronization, Frame Pattern and Viterbi
Signal Quality Status: Eb/No, Deviation, Frame Sync Pattern Error Count, Viterbi Error Count
and BERT / PRN BER Measurements on Front Panel Display and Remote Port

Ordering Information

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MD2365-02	Basic Dual Channel Unit (20 Mbps)	OP2365-30	Rack Mount I/O Terminal
MD2365-04	Basic Quad Channel Unit (20 Mbps)	OP2365-40	Special Rear I/O
MD2365-01	Basic Single Channel Unit (20 Mbps)	OP2365-41	Recirculate (NRZ-L & Clk In/ RNRZ Out)
OP2365-01	Operation to 40Mbps	OP2365-43	BERT Option
OP2365-05	QPSK & OQPSK Support	OP2365-45	Auto Scan Option
OP2365-06	SOQPSK Support	OP2365-70	75 ohm option
OP2365-07	QPSK & OQPSK & SOQPSK	OP2365-91	Extended Loop Bandwidth Range
OP2365-21	IEEE-488 Remote Control	OP2365-92	Reed Solomon Option
OP2365-22	Ethernet Remote Control		

Recognizing that no standard product can meet all the needs of all users, GDP stands ready to provide units tailored to unique applications.

The statements in this data sheet are not intended to create any warranty, expressed or implied. Equipment specifications are subject to change without notice.

300 Welsh Road · Building 3 · Horsham, PA 19044-2273
Phone: 215-657-5270 Fax: 215-657-5273

URL: <http://www.gdpspace.com>
E-mail: gdpinfo@gdpspace.com